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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/707,844	11/08/2000	Hidetoshi Ishida	0819-448	9493

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EXAMINER

FINSMITH, DAVID C

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 12/19/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/707,844

Applicant(s)

MIYATSUJI ET AL.

Examiner

David C Finsmith

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 November 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 6 and 7 is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 Nov. 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

1. Claims 1 and 4 are rejected as unpatentable under 35 USC 102(a) as being anticipated by Aoyama et al (U.S. Patent Number 5,933,364).

Aoyama et al teaches a semiconductor device comprising a semiconductor substrate; at least two semiconductor components on the principal surface of the substrate; and multiple through holes, which pass from the principal surface through the backside of the substrate and are provided in a region of the substrate between the at least two components and a conductive film that is connected to a grounded wiring layer (see fig. 1 and column 4 lines 20-40 and figure 10 and column 9 lines 25-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al in view of Wolf.

Aoyama et al teaches as explained in paragraph 1.

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Aoyama et al does not teach that a device with a gap between 2 adjacent through holes or vias should be smaller than the thickness of the substrate so the semiconductor structure will not easily fall apart and will keep the device to a minimum size.

Wolf teaches that the gap between 2 adjacent through holes or vias should be smaller than the thickness of the substrate so that the semiconductor structure will not easily fall apart and will keep the device to a minimum size (see Silicon Processing Volume 2 by Wolf page 243).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the through holes of the device of Aoyama et al a distance apart less than the substrate thickness in view of the Wolf teaching as explained above.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al in view of Dawson.

Aoyama et al teaches as explained in paragraph 1

Aoyama et al does not teach filling the sides of the through holes with a conductive material.

Dawson teaches filling the sides of the through holes with a conductive material (see Column 4 lines 20-27) to increase the devices tolerance to electrostatic discharge and electromagnetic interference.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to fill the sides of the through holes of the device of Aoyama with a

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conductive material as in the device of Dawson to improve the devices tolerance to electromagnetic interference and electrostatic discharge.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama et al in view of Schmitz et al (U.S. Patent Number 6,313,512).

Aoyama et al teaches as explained in paragraph 1 above.

Aoyama et al does not teach the device is a power amplifying transistor for a radio frequency signal.

Schmitz et al teach a semiconductor device that is a power amplifying transistor for a radio frequency signal (see column 1 lines 1-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine two or more of the devices of Schmitz et al in the device of Aoyama et al because one could reasonably expect to obtain a compact radio frequency amplifier that has improved electrostatic discharge and improved electromagnetic interference tolerance.

Allowable Subject Matter

Claims 6 and 7 are allowable.

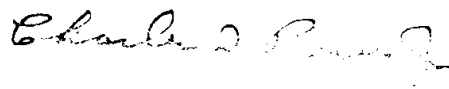
The prior art of record does not teach or suggest a semiconductor substrate having at least two semiconductor components on the principal surface of the substrate; electrodes of the at least two components provided on the substrate; a first group of

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holes, which pass from the principal surface through the backside of the substrate and are provided in respective regions of the substrate under the electrodes; a first conductor film provided on the side faces of the first group of through holes; a second group of holes which pass from the principal surface through the backside of the substrate and are provided in a region of the substrate between the components; A second conductor layer film provided on the side faces of the second group of through holes; and a wiring layer which is provided on the backside are of the substrate and is in contact with the first and second conductor films. The second conductor layer film and the wiring layer on the backside in contact with both the first and second layers is novel and the prior art does not describe the invention as claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David C Finsmith whose telephone number is 703-308-0121. The examiner can normally be reached between 8 A.M.-5 P.M. from Monday – Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers can be reached on 703-308-2417. The fax phone numbers for TC 2800 where this application is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-6785.

D.F. November 28, 2001



Supervisor
Technology Center